A GaN based Doubly Grounded, Reduced Capacitance Transformer-less Split Phase Photovoltaic Inverter with Active Power Decoupling

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Abstract—Transformer-less PV inverters are gaining widespread applications with lower cost, reduced footprint, and improved efficiency. This paper proposes a topology that can eliminate the common mode leakage current which is a major challenge in transformer-less PV inverters. In addition, an active power decoupling strategy is implemented in this topology instead of using large energy storage element for double line frequency power decoupling which is a common problem in single phase inverters/rectifiers, thus achieving a smaller volume and replacing electrolytic capacitors with film capacitors to increase reliability. A constant input voltage with negligible double line frequency ripple component less than 2% ensuring high MPPT efficiency is achieved in this topology through control strategy. Compared with previous topology, the 120 Hz inductor current ripple in the boost stage is reduced significantly resulting in the decrease of the RMS current value by 14% and the peak current value by 41%. Also the RMS current in the input capacitor is decreased by 91%. The dc link capacitor volume is also decreased with the increase of the voltage level. Finally, a 1 kW, 100 kHz single-phase prototype with 200 V DC nominal input and 120 V/60 Hz AC output in split phase configuration using GaN FETs has been built to validate the theoretical analysis. The control strategy and modulation scheme are implemented in DSP TMS320F28335.

Keywords—PV inverter, doubly grounded, leakage current, power decoupling, split phase

I. INTRODUCTION

Photovoltaic (PV) source nowadays is taken as one of the most promising renewable energy sources since it has many advantages such as clean, reliable and emission free [1]. Power density and efficiency are becoming more and more important metrics recently to achieve smaller volume, lighter weight and improved performance with the fast development of wide bandgap devices, new topologies and advanced control method (WBG) [2-7]. Transformer-less PV inverters, with higher power density, lower cost and improved efficiency, are gaining widespread applications compared to the ones with transformer galvanic isolation as a result [8].

A key issue with the transformer-less inverters approach is the presence of the common mode leakage current (ground current) which can increase the system loss, cause safety issue and induces EMI problem [9]. The full bridge inverter with bipolar sinusoidal pulse width modulation scheme (SPWM) can be potential candidates as the high frequency common mode voltage is always a constant value resulting in little leakage current problem. Other more involved solutions present relatively complex topologies such as the HERIC, H5, H6 with ac bypass, or H6 with dc bypass [10-13]. All these proposed configurations are able to effectively address the common mode leakage current problem but come with the drawbacks of more number of active or passive components or requirement of some complex control strategies. The converter in [14] is a combination of a bidirectional buck-boost converter and two half-bridge split phase inverters but the filter components used are bulky resulting in lower power density.

Another challenge with the single phase inverters/rectifiers is the presence of the double line frequency power ripple [15-16] that needs to be supported by some energy storage components. An extensive research has already being conducted in the direction of decreasing the requirement of the capacitance for the power decoupling so that the volume of the decoupling capacitor can be significantly decreased and the electrolytic capacitor which presently dominates the power decoupling approach can be replaced by film capacitor which has a longer lifetime and is more reliable [17]. Some converters address the issue by adding an additional conversion stages (an auxiliary circuit) to handle the double line frequency ripple power which can be connected in either series or parallel to the primary converter [15-21]. The main disadvantages of such approaches are the complex circuit, higher cost and more number of components which will bring down the efficiency. They also have to encounter higher current stress on the auxiliary circuit if connected in series or higher voltage stress if connected in parallel. Some implement sophisticated control schemes without affecting the power quality or implement the power decoupling scheme with reduced number of active components but could not effectively decrease the capacitance requirement [19-21].

In this paper, a transformer-less PV inverter is proposed to effectively address the leakage current problem and 120 Hz power decoupling problem at the same time. High power density is achieved by reduced volume of both decoupling capacitors and filter inductors (by increasing the switching frequency with GaN switches). The control strategy of the proposed circuit is analyzed and the advantages of the
proposed topology are shown. A 3 kW single-phase prototype with 200 V DC nominal input and 120 V/60 Hz AC output in split phase configuration using GaN FETs is built and tested. Simulations results and their corresponding experimental results are presented to validate the theoretical analysis.

II. PROPOSED TOPOLOGY AND CONTROL SCHEME

Fig. 1 shows the topology which consists of a boost stage and half bridge stages connected in split phase configuration which is the variation of the topology proposed in [14]. The left part is the boost stage that controls the dc link voltage \( V_{\text{link}} \) to be around twice the input voltage \( V_\text{in} \) which represents the PV panel voltage. \( V_\text{in} \) and \( V_{\text{link}} - V_\text{in} \) form the two dc sources or voltage levels for the half-bridge inverter stage that controls the ac output voltage and shown at the right in Fig. 1. The input voltage \( V_\text{in} \) is controlled to have negligible double line frequency ripple. The dc link voltage \( V_{\text{link}} \) is almost twice of the input voltage to supply sufficient voltage for the grid voltage modulation.

Due to the doubly grounded structure (the connection of the negative terminal of the PV panel and grid), there is little common mode leakage current which usually is a huge problem in the transformer-less PV string inverters.

The dc link capacitor \( C_{\text{link}} \) will be used to decouple the 120 Hz power. Compared to the topology proposed in [14], the dc link capacitor \( C_{\text{link}} \) in this paper is placed directly across the positive terminal and negative terminal to increase the voltage level of the capacitor and therefore decrease the capacitor volume [22]. Apart from the topology improvement, instead of using 1.2 kV SiC switches as implemented in [14] which has too much voltage margin, 650 V GaN HFETs are used to improve the efficiency and get better circuit performance for the same application.

Fig. 1 shows the control strategy for the proposed topology in Fig. 1. \( V_\text{in} \) that represents the PV panel voltage and \( V_{\text{link}} - V_\text{in} \) that is generated by the left dc-dc boost stage form 2 dc sources that will fulfill the modulation for the output voltage in standalone configuration or the output current in grid connected configuration. The PV panel voltage \( V_\text{in} \) is controlled to have negligible ripple to achieve high MPPT efficiency by using PR controller resonant at 120 Hz, and therefore, all the 120 Hz power component is supported by dc link capacitor \( C_{\text{link}} \). The dc link voltage \( V_{\text{link}} \) average value is controlled by using a low bandwidth Butterworth filter and the output is the grid current magnitude reference which will then be used to regulate the grid current and therefore the power.

For the modulation requirement the following relationships of (1) always need to be satisfied to generate the output sine waves and similar requirement is true for the second phase. (2) shows the decoupling capacitance relationship and can be used to calculate the decoupling capacitance needed.

\[
\begin{align*}
V_\text{in} &> V_{g1} & V_{g1} &> 0 \\
V_{\text{link}} - V_\text{in} &> -V_{g1} & V_{g1} &\leq 0
\end{align*}
\]

(1)

\[
C_{\text{link}} = \frac{S}{\alpha h V_{\text{link}, \text{avg}} V_{\text{link}, \text{pk-pk}}}
\]

(2)

III. ANALYSIS OF OPERATION AND SIMULATION RESULTS

The operation of the proposed inverter will be analyzed and salient simulation waveforms in PLECS will be shown. Simulation results are in standalone case with resistive load. To simulate the PV panel, a constant dc voltage source of 270 V will 5 ohm resistor is used.

Table I shows the specifications used in simulation as well as the designed hardware of the proposed topology. Table II shows the details of the components used for the proposed topology. The dc link capacitance is around 40 uF, 550 V / kW allowing 150 V pk-pk ripple in the dc link voltage and the max dc link voltage is 510 V which is limited by the GaN FETs voltage ratings. Also the input capacitance is very small which is only 3 uF.

<table>
<thead>
<tr>
<th>Table I: Main circuit specifications</th>
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<tbody>
<tr>
<td><strong>Power</strong></td>
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<tr>
<td><strong>DC input voltage</strong></td>
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<tr>
<td><strong>Load voltage</strong></td>
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<tr>
<td><strong>Load current</strong></td>
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<tr>
<td><strong>Power factor</strong></td>
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<td><strong>Carrier frequency</strong></td>
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<table>
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<tr>
<th>Table II: Components details</th>
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<tbody>
<tr>
<td><strong>DC link capacitance (C_{\text{link}})</strong></td>
</tr>
<tr>
<td><strong>DC input capacitance (C_{\text{in}})</strong></td>
</tr>
</tbody>
</table>
### Inverter side inductor ($L_{inv}$)
210 uH

### Boost side inductor ($L_b$)
210 uH

### Switch
650V GaN System FET GS66516T

### Inductor
Planar Ferrite Core 3C94 with Litz Wire

Fig. 3 shows the simulation waveforms of the proposed topology. The output voltages are sinusoidal waveforms. The input voltage is controlled to be with extremely small ripple (less than 2% of the input voltage average value). The dc link voltage has large 120 Hz ripple which will decouple the 120 Hz power.

![Fig. 3 Dc link voltage, input voltage and grid voltages](image)

Fig. 4 shows the duty cycle of the boost stage and inverter stages from which it can be seen that due to the 120 Hz large swing in the dc link voltage, all duty cycles need to contain 120 Hz information to maintain the input voltage to be a pure dc and output voltage to be perfect sinusoidal waveforms which is achieved by good designed controllers.

![Fig. 4 Boost stage duty cycle and inverter stage duty cycles](image)

Fig. 5(a) shows the boost stage inductor current waveforms of the proposed topology. It can be seen that unlike the topology in [14] where the inductor current in dc-dc stage has large 120 Hz ripple as shown in Fig. 5(b), the boost inductor current of the proposed topology is merely a pure dc with switching frequency ripple. Compared with previous topology in [14], the 120 Hz ripple component in the boost inductor current is reduced significantly resulting in the decrease of the RMS current value by 14% and the peak current value by 41%.

![Fig. 5 Boost inductor current, input current and inverter inductor currents](image)

Fig. 6(a) shows the input capacitor current of the proposed topology. As the dc-dc stage is inherently a boost stage which consists of a boost inductor at the input, the current ripple at the input capacitor is very small. Fig. 6(b) shows the input capacitor current of the topology in [14]. Due to the topology difference, the dc-dc stage is a buckboost stage resulting in large current ripple in the input capacitor. The decrease of the RMS current in the input capacitor is 91% compared to the topology in [14]. The input current is clean in the proposed
topology and the input current in [14] contains large amplitude of switching frequency ripple which needs much larger input capacitor to filter which is the inherent disadvantage of the buckboost topology.

The topology in [14] Fig. 6 Input capacitor current

![Input capacitor current (iCin)](image)

(a) Proposed topology

![Input capacitor current (iCin)](image)

(b) The topology in [14]

Fig. 6 Input capacitor current

IV. HARDWARE IMPLEMENTATION AND RESULTS

A 3 kW inverter using the proposed topology with LC filter and resistive load in standalone mode operating at 100 kHz switching frequency has been built to validate the proposed topology and corresponding benefits. All the components in Table II are designed for 3 kW operation while the experiment by far is done up to 1 kW (full voltage, 1/3 load current). The experiments at 3 kW will be conducted in the later work.

Fig. 7 shows the hardware prototype. 650 V GaN FETS GS66516T with 27 mohm $R_{ds}$ from GAN SYSTEM are used for all the switches. A 230 V constant dc voltage source and a 5 ohm resistor in series are used to simulate the PV panel. The driver ICs are chosen as Silicon Labs Si8271. The positive gate voltage of the MOSFET ($V_{gs}$) is 6.5 V and the negative is 0 V. LeCroy 6200A oscilloscope is used to capture waveforms. Power analyzer YOKOGAWA WT3000 is used to measure the efficiency. Inductors are built by hand using Ferrite core 3C94 with Litz wire [23]. The TI DSP TMS320F28335 is used for control.

![3 kW hardware prototype of the proposed topology](image)

Fig. 7 3 kW hardware prototype of the proposed topology

Fig. 8 shows the experiment waveforms of the proposed topology. It can be seen that the output voltage are sinusoidal waves with THD < 2%. The dc link voltage is controlled to vary a lot which decouples the 120 Hz power. The input voltage ($v_{in}$) and the difference between the dc link voltage and the input voltage ($v_{link} - v_{in}$) need to be both larger than the grid voltages as analyzed in (1) to ensure that the voltage modulation has enough margin and the output voltages are not distorted.

![Waveforms of dc link, input and output voltages in standalone mode](image)

Fig. 8 Waveforms of dc link, input and output voltages in standalone mode (time scale 5 ms/div, all voltages scale 100 V/div)

Fig. 9 shows the 120Hz ripple of the input voltage and current which is closely related to the MPPT efficiency. The input voltage is controlled to be with very small ripple (1.9% of the input voltage RMS value) and due to the 5 ohm resistor connected with the input dc voltage source to simulate the PV panel, the input current has a correspondingly 13% 120 Hz
ripple of the input current RMS value. The boost inductor current is almost just a dc offset which is equal to the input current with some switching frequency ripple. The experiment waveforms match with the simulation results very well.

Fig. 9 120 Hz ripple of input voltage and current (time scale 5 ms/div, V_in scale 100 V/div, i_in scale 10 A/div, i_b scale 5 A/div)

Fig. 10 shows the duty cycle of boost stage and inverter stages from which it can be seen that to maintain a dc input voltage the duty cycle of the boost stage needs to contain some 120 Hz information. Also to have a sinusoidal output voltage the inverter stages duty cycle need to have 120 Hz information too which come from the output of the high bandwidth controllers.

The overall efficiency of the proposed inverter at 1 kW is 95.1% at 100 kHz and 95.6% at 75 kHz. As the components and parameters are designed for 3 kW (GaN FETs are chosen with low R_ds(ON) which is 27 mohm), the efficiency value which is currently a little low has the potential to be improved at full power. Also the gate resistance now used is large (on resistance 20 ohm and off resistance 5 ohm). The designed efficiency at 3 kW is larger than 97.5% and the experiments at 3 kW with methods to improved efficiency will be conducted in the future work.

V. CONCLUSION

This paper proposes a topology that can eliminate the common mode leakage current which is a major challenge in transformer-less PV inverters. An active power decoupling strategy is implemented instead of using large energy storage element for 120 Hz power decoupling, thus achieving a smaller volume. A constant input voltage with negligible double line frequency ripple component (less than 2% of the average value) ensuring high MPPT efficiency is achieved. Compared with previous topology, the boost inductor current 120 Hz ripple is reduced significantly to decrease the current RMS value 14% by and the peak value by 41%. Also the RMS current in the input capacitor is decreased by 91%. The dc link capacitor volume is also decreased with the increase of the voltage level. A 1 kW, 100 kHz single-phase prototype with 200 V DC input and 120 V/60 Hz AC output in split phase configuration using GaN FETs has been built to validate the theoretical analysis. The control and modulation scheme are implemented in DSP TMS320F28335.

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